Energy-aware scheduling under topological constraints

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High Performance Computers (HPCs) are widely used to run applications of great societal importance, due to their extreme computational power. Since their debut, the goal of engineers as well as of the scientific community is to increase their efficiency. For many years, this was achieved via the hardware of the systems: either by increasing the scale of the platform, or by introducing special purpose processors and heterogeneity on the machines (nodes), or by improving the interconnection network. However, when the energy consumption limit was met, HPCs' designers turned their focus on the scheduling algorithms.

Nowadays, real life HPCs consist of more than one type of nodes like computational accelerators (GPUs) as well as machines dedicated to the communication with the file system (Input/Output nodes). GPUs are used due to their computational efficiency in specific kind of operations while I/O nodes have a positive effect on reducing communication cost and they can prevent the network from acting as a bottleneck to the overall performance of the platform, since a single all-purpose interconnection network is usually implemented in a HPC platform.

As the complexity of platforms increases, the need for new, more precise, platform-oriented algorithms, which take into consideration the various features of HPCs, is crucial.

Bleuse et al. (EuroPar 2018) [1] introduced a general model for interference-aware scheduling in large scale parallel platforms. They considered two different types of communications: the flows induced by data exchanges during computations and the flows related to Input/Output operations. Rather than taking into account these communications explicitly, they restrict the possible allocations of a job by external topological constraints. In their work, jobs are considered to be rigid: a job requires a specific number of machines as well as a prespecified Input/Output processor in order to be executed. Here, we propose to adopt the same framework for the platform and the aforementioned topological constraints, but to extend their study by taking explicitely into account the energy consumption. For that, we plan to adopt the *speed scaling* model. In the *speed scaling* model [2], the speed of the processor (machine) may be dynamically changed over time. When a processor runs at speed s, then the rate with which the energy is consumed (i.e., the power) is $f(s)$ with f a non-decreasing function of the speed. The energy is the integral of the power over time. According to the well-known cube-root rule for CMOS devices, the speed of a device is proportional to the cube-root of the power and hence $f(s) = s^3$, but in the literature, many works consider that the power is $f(s) = s^\alpha$ where $\alpha > 1$ is a constant, or an arbitrary convex function. Many scheduling problems have been studied in this model and recently, Kononov and Kovalenko [3] considered the case of rigid parallel jobs. We propose to first extend his study by introducing Input/Output nodes as in the model of Bleuse et al. [1].

The student will have to first study the related bibliography and then to design and evaluate efficient algorithms for the problem. The evaluation may be either analytical and/or using simulations.

References

[1] Raphaël, Bleuse Konstantinos Dogeas, Giorgio Lucarelli, Grégory Mounié, Denis Trystram, Interference-Aware Scheduling Using Geometric Constraints. 205-217 2018 Euro-Par

[2] F. Frances Yao, Alan J. Demers, Scott Shenker, A Scheduling Model for Reduced CPU Energy. 374-382 FOCS, 1995

[3] Alexander V. Kononov, Yulia V. Kovalenko Approximation algorithms for energy-efficient scheduling of parallel jobs. 693-709 2020 23 J. Sched.